

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	("(gatewith(controlfloating)) withmemory").PN	US-PGPU B; USPAT; EPO; JPO	OR	OFF	2004/12/01 13:35
L2	0	(gate with (controlfloating)) with memory	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:36
L3	30062	(gate with (control floating)) with memory	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:36
L4	22375	3 and (source drain)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:38
L5	13304	4 and (stack\$3 wordline word adj line)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:37
L6	3904	5 and ((source drain) with (contact\$3 stud plug pillar))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:39
L7	3927	5 and ((source drain) with (contact\$3 stud\$3 plug pillar))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:39
L8	3893	7 and (dielectric insulat\$3 conduct\$4 oxide polysilicon)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:42
L9	1097	8 and ((silicide salicide metal adj refractory) with (gate source drain))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:47
L10	1028	9 and (trench hole via hole opening)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 13:48
L11	988	10 and (silicide with (source drain plug contact stud gate))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 14:03
L12	470	11 and (silicide with (control adj gate))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 14:04
L13	170	12 and (silicide with (source drain))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/01 14:05

L14	1	"6387784".PN.	USPAT; USOCR	OR	ON	2004/12/01 14:43
L15	1	"6159800".PN.	USPAT; USOCR	OR	ON	2004/12/01 14:43
L16	1	"6103576".PN.	USPAT; USOCR	OR	ON	2004/12/01 14:44
L17	1	"5521108".PN.	USPAT; USOCR	OR	ON	2004/12/01 14:44
L18	1	"4775642".PN.	USPAT; USOCR	OR	ON	2004/12/01 14:44

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Active

- L3: (30062) (gate with (control floating)) with memory
- L4: (22375) 3 and (source drain)
- L5: (13304) 4 and (stack\$3 wordline word adj line)
- L6: (3904) 5 and ((source drain) with (contact\$3 stud plug pillar))
- L7: (3927) 5 and ((source drain) with (contact\$3 stud\$3 plug pillar))
- L8: (3893) 7 and (dielectric insulat\$3 conduct\$4 oxide polysilicon)
- L9: (1097) 8 and ((silicide salicide metal adj refractory) with (gate source drain))
- L10: (1028) 9 and (trench hole via hole opening)
- L11: (988) 10 and (silicide with (source drain plug contact stud gate))
- L12: (470) 11 and (silicide with (control adj gate))
- L13: (170) 12 and (silicide with (source drain))

12 and (silicide with (source drain))

USPGPUB USPAT EPC JPO

Default Extension: OR

Buttons: Browse, Clear, Search, Highlight all hit terms exactly

Buttons: EPS form, IS&P form, Image, Text, HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	J	A	
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20041023910A	20041118	34	Nonvolatile semiconductor memory and read method	365/222			Sato, Hiroshi et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20041023790	20041111	62	Semiconductor device	365/202			Shukuri, Shoji et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20041021420A	20041028	50	Nonvolatile semiconductor memory device and method	438/257			Shimizu, Shu	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20041020700	20041021	24	Two mask floating gate EEPROM and method of making	257/314			Kouznetsov, Igor G. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20041019561A	20040923	91	Semiconductor integrated circuit device and method	438/257			Shukuri, Shoji	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20041019561A	20040923	47	Nonvolatile memories and methods of fabrication	438/257	438/258		Ding, Yi	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20041017040A	20040916	71	Data writing method for semiconductor memory device	365/185.22			Noguchi, Mitsuhiro et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20041015009A	20040819	40	Method of manufacturing a semiconductor integrated circuit	257/331			Lee, Sang-Eun et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20041015009A	20040819	18	Non-volatile semiconductor memory device and method	257/315			Hakozaki, Kenji et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20041014500A	20040729	20	Non-volatile memory device having dual gates and method	257/321			Min, Hong-Kook et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20041012510A	20040715	16	Cell structure of non-volatile memory device and method	257/315			Lee, Tae-Jung et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
12	<input type="checkbox"/>	<input type="checkbox"/>	US 20041011010A	20040624	11	Non-volatile memory device having improved programming	257/315			Kang, Sung-Taeg	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
13	<input type="checkbox"/>	<input type="checkbox"/>	US 20040527	20040527	19	FOUR-BIT NON-VOLATILE	365/185.03			Rojzin, Yakov et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>



$\text{ZrL13, (170) 12 and (silicide with (source drain))}$ 

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DE: USPGPUB USPAT 580,180

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	3	4	5	6
21			US 20030000210	20031204	33	Semiconductor device and method of manufacturing the same	257/406	257/E29.165;		Tanaka, Masayuki et al.							
22			US 20030000447	20031106	63	Nonvolatile memory device and method of fabricating the same	365/185.33	257/E20.200;		Tuan, Hsing Ti et al.							
23			US 20030100006	20031023	92	Semiconductor integrated circuit device and a method of manufacturing the same	365/185.18	257/E21.625;		Shukuri, Shoji							
24			US 20030155650	20030821	24	Self-aligned split-gate flash memory cell and its controller	365/185.33	365/185.18		Wu, Ching-Yuan							
25			US 20030146455	20030807	15	Methods of forming memory cells and arrays having voided cells	257/213			Abedifard, Ebrahim							
26			US 20030142300	20030731	25	Methods of fabricating a stack gate flash memory array	438/197			Wu, Ching-Yuan							
27			US 20030120604	20030710	33	Nonvolatile semiconductor memory and read method	365/200			Sato, Hiroshi et al.							
28			US 20030120193	20030703	19	Contactless non-type memory array and its fabrication method	257/315	257/202;		Wu, Ching-Yuan							
29			US 20030111605	20030619	21	Semiconductor memory device with a silicide layer for contact	257/384	257/314;		Kanamori, Kohji							
30			US 20030000549	20030522	42	Semiconductor integrated circuit device	365/200	257/E21.69;		Ichige, Masayuki et al.							
31			US 20030000450	20030403	16	Process for manufacturing electronic devices comprising a semiconductor device	438/201	257/E21.645;		Grossi, Alessandro et al.							
32			US 20030000005	20030313	17	Method of manufacturing semiconductor devices	438/258	257/E21.688;		Nitta, Toshinari et al.							
33			US 20030000661	20030313	87	Nonvolatile semiconductor memory	365/185.14	257/E20.091;		Sakui, Koji et al.							
34			US 20030000006	20030213	6	STACKED-GATE FLASH MEMORY DEVICE	257/314	257/296;		Hsu, Scott							
35			US 20030000097	20030213	19	Semiconductor memory device	257/296	257/202;		Ooi, Makoto							
36			US 20030000661	20030102	11	Method of manufacturing semiconductor devices	438/258	257/E21.684;		Lee, Hee Youl							
37			US 20030140050	20021017	34	Integrated memory cell and method of fabrication	257/314	257/E21.162;		Fazio, Albert et al.							
38			US 20030142546	20021003	25	Two mask floating gate EEPROM and method of making the same	438/257	257/E21.165;		Kouznetsov, Igor G. et al.							
39			US 20030141240	20021003	71	Data writing method for semiconductor memory device	365/185.22	257/E20.100;		Noguchi, Mitsuhiro et al.							
40			US 20030141187	20020822	33	Nonvolatile semiconductor memory and read method	365/185.03			Sato, Hiroshi et al.							







2 L13. (170) 12 and (silicide with (source drain))

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7. **Answer: D**

☒ This is my final offer



